ITC 1.0 Radio Manufacturing Test Plan: Wayside, Base, and Locomotive

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Revision History

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1. Introduction

1.1 Purpose

This document outlines the test strategy and testing required for the ITC Wayside Radio, Base Radio, and the Locomotive Radio at the Contract Manufacturers (CM). The testing is based on demonstrating that each product shipped from the CM is properly configured and calibrated, meets product specifications, and is free of defects.

The primary purpose of the PCBA functional test system and unit test system is to support manufacturing; the secondary purpose is to support repair at the Railroad Central Repair Facilities (CRFs).

This is a living document; it will be updated periodically to reflect the work in progress with the CM and evolving test development.

1.2 Scope

This test plan addresses the testing of the UUT during and following the manufacturing process. The tests outlined with this document are intended to detect process problems within manufacturing. These tests are not intended to be “type” tests. (Note: Type tests are defined as tests, which are intended to be one-time test of a representative product that will be manufactured. Type tests are typically performed for either design verification or for certification evaluation). Therefore, embedded product software and algorithms are not tested by the test methods outlined within this test plan. However, the unit test does check functionality of the software in the product.

This test plan also addresses the equipment used to repair boards and radios at the CRFs.

1.3 References

Table 1: References

Description	Drawing Number
ITC Base Station Radio Product Description	00001064-A
ITC Locomotive Radio Product Description	00001065-A
ITC Wayside Radio Product Description	00001063-A
ITC 220MHz Radio Functional Product Specification – Product Release	00001056-A
ITC 220MHz Radio Hardware Specification – Product Release 1.0	00001040-A
ITC 220MHz Radio System Architecture Specification	00001049-C

1.4 Acronyms and Definitions

Table 2: Acronyms and Definitions

Acronym/Term	Term	Definition
AOI	Automated Optical Inspection	
AQL	Acceptable Quality Limit	
AXI	Automated X-Ray Inspection Laminography	
BOM	Build Of Material	
BST	Boundary Scan Test	
CM	Contract Manufacturer	
EMS	Electronic Manufacturing Services	
HW	Hardware	
ICT	In-Circuit Test	
IQA	Incoming Quality Assurance	
ITC	Interoperable Train Control	
MCC	Meteorcomm, LLC	

Acronym/Term	Term	Definition
MCC TE	Meteorcomm Test Engineering	
OBA	Out of Box Audit	
OEM	Original Equipment Manufacturer	
ORT	On-going Reliability Test	
PA	Power Amplifier	
PCBA	Printed Circuit Board Assembly	Same as PWA (Printed Wire Assembly)
PCBA-FT	PCBA Functional Test	
PCB	Printed Circuit Board	Same as PWL (Printed Wire List)
PEP	Peak Envelope Power	
POST	Power On Self Test	
PWA	Printed Wire Assembly	
PCA	Printed Circuit Assembly	
QA	Quality Assurance	
SW	Software	
TBD	To Be Decided	
TE	Test Engineering	
TCXO	Temperature Compensated Oscillator	
UUT	Unit Under Test	

1.5 Product Overview

The products to be manufactured and tested at the CM will be the Wayside Radio, Base Radio, and the Locomotive Radio.

1.5.1 Major Components

Table 3: Product Component Summary

Product	ID	Major Components	Notes
Wayside Radio	1	Master PCBA	Different bare board than Base and Locomotive Radio
	2	T-R Switch/LPF PCBA	
	3	RF/DC Power PCBA	13.6VDC Input
	4	RF PA Module	Module mounted on the chassis
Base Radio	1	*Master PCBA	Uses same bare board as Locomotive with different component stuffing option.
	2	Front End PCBA	
	3	PA-Mod PCBA	
	4	*LED PCBA	Uses same bare board as Locomotive
	5	Ethernet PCBA	Final assembly uses two
	6A	24V Power Supply Assembly	Base Radio is assembled with either 24VDC or 48VDC supply.
	6B	48V Power Supply Assembly	
Locomotive Radio	1	*Master PCBA	Uses same bare board as Base Radio with different component stuffing option.
	2	Front End PCBA	
	3	PA-Mod PCBA	
	4	*LED PCBA	Uses same bare board as Base Radio
	5	Power Supply	+74 VDC Input

* Bare board is common in Base and Locomotive Radio with different BOM.

2. Test Strategy

The test strategy for the ITC Wayside Radio, Base Radio, and the Locomotive Radio is based on demonstrating that each product shipped to our customers is properly configured and calibrated, meets product specifications, and is free of defects. To achieve this strategy, several test schemas are integrated in a hierarchy fashion progressing from the component level to the system level as the product passes through the production process phases.

Appropriate test locations will be identified within the production flow to define the optimum combination of tests to apply. The objective is to detect faults at the lowest possible level, preventing defects from reaching the next assembly, where detection is more difficult and the consequences of failure more severe.

2.1 Test Team

2.1.1 Test Team Composition

Manufacturing test systems will be developed by a team composed of MCC, CM, and third party test system vendor personnel. While all parties will share accountability for various aspects of the project, ultimate ownership and leadership will reside with MCC personnel.

- MCC Test Engineering will own all Manufacturing Test Specification (MTS) documents.
- MCC Test Engineering will oversee test engineering activities and manage the overall project.

2.1.2 Test Team Roles and Responsibilities

All team members will work together to architect an end to end solution that best meets the project's needs, given all schedule, budget, and technical considerations. Project needs will be evaluated against the known available resources at MCC, CMs, contractors and third party vendors. A gap analysis will be provided to map residual open areas to new resources.

- All MCC personnel will work together to manage a host of outside resources working on each test stage to help with test system HW/SW development, documentation, etc.
- ICT: CM will provide primary development, with consulting from a third party expert if needed. This includes JTAG Boundary Scan test development at ICT and on a standalone bench.
- PCBA FT: Vendor will perform detailed design under MCC direction.
- Unit Test, Stress Screen, Out of Box Audit (OBA), On-going Reliability Test (ORT): Vendor will perform detailed design under MCC direction.

- SW development will be performed by the Vendor under MCC direction.

Table 4: Test Activities and Deliverables

Test	Team	Activities	Deliverables
Bare Board Testing	CM Board house	CM will coordinate board house to have 100% bare board test. CM will coordinate board house to implement controlled impedance testing on a QA sample.	Boards are tested prior to component placement.
AOI	CM	CM develops AOI testing and data collection system.	AOI test and data collection in place at factory.
AXI	CM	CM develops AXI testing and data collection system.	AXI test and data collection in place at factory.
IQA	CM	CM may develop tests for subassemblies if needed. CM finds location to archive C of C.	Established IQA Inspection in place at factory.
Programming Devices	CM	For initial build, CM to develop programming stations to program boards prior to PCBA-FT. In established production line, CM will have in-line programming capability or have preprogrammed CPLD & FLASH memory prior to attachment to bare board.	Programming stations ready for preproduction build. Preprogrammed CPLD & FLASH memory used for board assembly in established production line.

Test	Team	Activities	Deliverables
ICT and Boundary Scan Test (BST)	CM	ICT Fixture Build is outsourced. CM generates ICT test program for shorts, opens, components, etc. JTAG Boundary Scan to be integrated into ICT test program if practical.	ICT Test and data collection in place for preproduction build. Goal is to have JTAG BST available at this time.
	MCC Test Engineer and Development Engineer	Assist CM on how to properly powering up the Master board in ICT test and developing test(s) in ICT environment.	Standalone station for JTAG Boundary Scan Testing. JTAG Boundary Scan test is integrated into ICT test if practical.
	Engineer with JTAG Boundary Scan Expertise	Develops JTAG BST for Wayside, Base, and Locomotive Radios. Assist CM with the integration of JTAG Boundary Test into ICT.	
PCBA-FT	Vendor HW & SW Engineers RF Engineers	Build automated test system using off the shelf equipment and test software. Automated test system needs to be developed using older PCBA versions. Automated test system will be validated during preproduction build.	PCBA-FT and data collection in place for preproduction build. PCBA-FT to be validated during preproduction build. BOM, schematics, software, and documentation on building PCBA-FT testers.
	MCC Test Engineer and Development Engineer	Outlines test and methodology to be performed at PCBA-FT Test. Assist CM on how to control the Master board in PCBA test and developing tests. Assist CM on PCBA setup for testing.	
Hipot Test and Ground Bond Test	Vendor	Develops Hipot test for Locomotive Radio. Develops Ground Bond Test. These may be manual tests.	Hipot/Ground Bond Test and data collection in place for preproduction build.
	MCC Test Engineer	Outlines test and methodology to be performed at Hipot Test and Ground Bond Test. Assist in Hipot and Ground Bond Test development.	

Test	Team	Activities	Deliverables
Unit Test	Vendor HW & SW Engineers RF Engineers	Build automated test system using off the shelf equipment and test software. Automated test system needs to be developed using older radio version. Automated test system will be validated during preproduction build.	Unit Test and data collection in place for preproduction build. Unit Test to be validated during preproduction build. BOM, schematics, software, and documentation on building Unit Test testers.
	MCC Test Engineer and Development Engineer	Outlines test and methodology to be performed at Unit Test. Assist CM on how to control the UUT and developing tests. Assist CM on UUT setup for testing.	
Environmental Stress Screen (ESS)	CM	Implement Stress Screen using test system using off the shelf equipment and test software. Automated test system needs to be developed using older radio version. Automated test system will be validated during preproduction build.	Stress Screen and data collection in place for preproduction build. Stress Screen to be validated during preproduction build. BOM, schematics, software, and documentation on building test system used in Stress Screen.
	MCC Test Engineer and Reliability Engineer	Outlines test and methodology to be performed at Stress Screen. Assist CM on how to control the UUT and developing tests. Assist CM on UUT setup for testing.	
Out of Box Audit (OBA)	CM	Develop OBA with MCC Test Engineer.	OBA and data collection in place for preproduction build. OBA to be validated during preproduction build.
	MCC Test Engineer	Outline initial tests for OBA and work with CM to develop a final version.	

Test	Team	Activities	Deliverables
Ongoing Reliability Test (ORT)	CM	Implement ORT plan. This may require the use of equipment (such as shake table) not available on site. CM will coordinate ORT testing with outside HASA lab. Automated test system needs to be developed using older radio version. Automated test system will be validated during preproduction build.	ORT and data collection in place for preproduction build. ORT to be validated during preproduction build. ORT to be performed at both CM and HASA Lab (if required). BOM, schematics, software, and documentation on building test system used in ORT.
	HASA Lab	Run ORT tests with equipment not available at CM (e.g. shake table).	
	MCC Test Engineer and Reliability Engineer	Outlines test and methodology to be performed at ORT. Assist CM on how to control the UUT and developing tests. Assist CM on UUT setup for testing.	

2.2 General Requirements

2.2.1 Test System General Requirements

- Test systems will be developed and implemented concurrent to the product development.
- Test systems will use off the shelf equipment and software.
- Test system design will be robust. All cables used for interfacing the UUT to the test system can be easily replaced without opening the test system.
- Test Equipment used in measurements should be designed for a minimum Test Accuracy Ratio, TAR, (Spec tolerance/Test Equipment Accuracy) of 10.

- Example: Voltage regulator is 5.00 V +/- 10%, a DMM with a 1% accuracy or better is used to make this measurement. TAR = 10/1 = 10.
- Guard banding must be used for TAR between 4 and 10. For example: 5.00 V +/- 1%, a DMM with a 1% accuracy cannot met 10, then guard banding must be used to tighten the test limit.
- If a TAR < 4 is not easily achieved, exceptions may be allowed with MCC approval and documented.

- Test System Documentation should be in a hierarchical approach to facilitate ease of readability and to facilitate easy duplication of Test System.
  - Complete BOMs with long lead items marked.
  - Mechanical drawings.
  - Schematics
  - Calibration/Verification procedures
  - Equipment installation qualification procedure
  - Software and development environment
- Test System Validation report should include the following:

Requirements and Test Limit Verification

- Verify operator needs to be trained and certified.
- Verify tests are checked against MCC Manufacturing Test Specification (MTS). This can be captured by a traceability matrix.
- Verify instrument accuracy and range meets the test limit tolerance (i.e. TAR > 10).
- Order of test steps is adequate to produce good units.

Equipment Installation/Qualification

- Calibration, verification, maintenance documentation is released.
- Specifications and drawings for test equipment and fixtures are released.
- Software is released.

Performance Qualification

- Test system, test equipment, and test fixtures are calibrated and under calibration control.
- Test system is executing correct software revision and configuration.
- Verify integrity of automated test measurement with external test equipment.
- Verify Repeatability & Reproducibility – Gage Repeatability and Reproducibility (GRR) – consider sample size, Pass/Fail criteria.
- Verify Test Challenge – Verify Test system can identify failures (fault insertion).
- Verify Test system does not damage UUT.

- Test equipment capacity will be provided to meet the needs defined in the capacity summary section.
- All Test data (e.g. manual and automated tests) will be captured electronically. Test data will include operation, test steps, values, pass/fail, test system ID, test operator ID, pallet ID (as applicable), etc.
- CM Shop Floor Control will control the flow of product through Work In Progress (WIP).
- Verify Product handling equipment (trays to hold unit in place during test) does not cause scratches or cosmetic damage.

2.2.2 Assumptions

- PCBAs and Radio units are available for test development.
- CM will use older PCBAs and Radios F1/F2 versions for initial test development.
- PCBA CAD and assembly drawings are available for AOI, AXI, ICT and Board Functional Test development. Assembly drawings and product specifications are available for Unit Test.

2.3 Return and Repair (RnR) / Central Repair Facilities (CRFs)

2.3.1 Return and Repair (RnR)

The returns process will not be available at production launch. The remanufacturing processes may be developed after initial production launch. The CM will determine Remanufacturing devices will be sent to the production area where they will be disassembled or reassembled, as necessary, on a dedicated remanufacturing station. The CM Manufacturing Engineering will establish processes for handling returned new and used products.

2.3.2 Central Repair Facilities (CRFs)

Test systems for PCBA Functional Test and Unit Test can be used to support the Railroad Central Repair Facilities (CRFs). This will ensure that the boards and radios have the same level of production quality testing after being repaired.

3. Manufacturing Test Descriptions

The primary purpose of the identified test methods is to provide information about the manufacturing process. Each test method will accomplish this as follows:

3.1 Incoming Quality Assurance

Performed at: The CM

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM

Incoming Quality Assurance (IQA) tests certain received components and sub-assemblies to assure they are within manufacturer's specifications. This testing is typically performed on a sample Acceptable Quality Limit (AQL) basis. Alternately, IQA may receive tested components from manufacturers with a Certification of Compliance (C of C) or Certification of Analysis (C of A) providing proof of testing. CM must have a data retention plan that MCC reviews.

3.1.1 Wayside Radio

- Tested RF PA Modules, with C of C and test data for each module, shall be provided by the vendor. The C of C and test data will be archived.

3.1.2 Base Radio

- Tested DC to DC Power Modules (24 VDC=>28 VDC), with C of C and test data for each module, shall be provided by the vendor. The DC to DC Power Modules are used in the 24V Power Supply board. The C of C and test data will be archived.
- Tested DC to DC Power Modules (48 VDC=>28 VDC), with C of C and test data for each module, shall be provided by the vendor. The DC to DC Power Modules are used in the 48V Power Supply board. The C of C and test data will be archived.

3.1.3 Locomotive Radio

- Tested DC to DC Power Modules (72 VDC=>28 VDC), with C of C and test data for each module, shall be provided by the vendor. The DC to DC Power Modules are used in the Power Supply board. The C of C and test data will be archived.

3.2 Test Summary

Table 5: Summary of Tests

		Certificate of Compliance	Bare Board Electrical Net (100% sample)	Controlled Impedance (AQL% sample)	*Automated Optical Inspection (AOI) (100% sample)	*Automated X-Ray Inspection (AXI) (100% sample)	*ICT and Boundary Scan (100%)	PCBA Functional Test (100%)	Hipot Test (100%)	Ground Bond Test (100%)	Unit Test (100%)	Environmental Stress Screen(ESS) (AQL % sample)	Out of Box Audit (OBA) (AQL % sample)	On-going Reliability Test (ORT) (AQL % sample)
ID	**Major Components**													
	Wayside Radio													
1	Master PCBA		X	X	X	X	X	X						
2	T-R Switch/LPF PCBA		X	X	X			X						
3	RF/DC Power PCBA		X	X	X			X						
4	RF PA Module	X												
5	Final Assembly									X	X	X	X	X
	Base Radio													
1	Master PCBA		X	X	X	X	X	X						
2	Front End PCBA		X	X	X			X						
3	PA-Mod PCBA		X	X	X			X						
4	LED PCBA		X	X	X			X						
5	Ethernet PCBA		X	X	X			X						
6A	24V Power Supply PCBA		X	X	X			X						
6B	48V Power Supply PCBA		X	X	X			X						
7	Final Assembly									X	X	X	X	X
	Locomotive Radio													
1	Master PCBA		X	X	X	X	X	X						
2	Front End PCBA		X	X	X			X						
3	PA-Mod PCBA		X	X	X			X						
4	LED PCBA		X	X	X			X						
5	Power Supply		X	X	X			X						
6	Final Assembly								X	X	X	X	X	X

Notes:

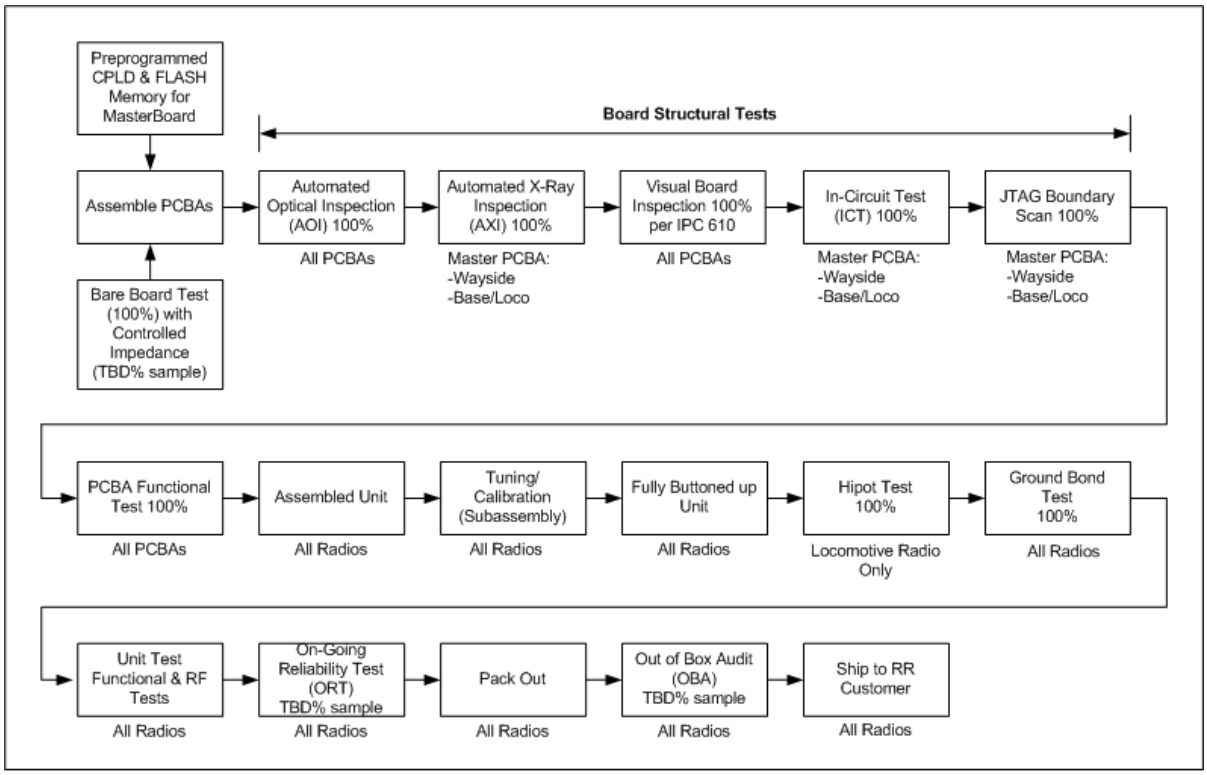
1) * AOI, Xray, and ICT to be balanced for test coverage for PCBA structural defect coverage.

2) 3D X-Ray for BGAs and similar devices only

3) Master PCBAs to get ICT testing 100%, including JTAG

4) All connectors and indicators must be tested at the device level for proper function

Figure 1: Product Flow Chart



3.3 Bare Board Testing

Performed at: The CM/OEM board supplier's factory

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM or OEM board supplier

- Testing is performed on all bare boards to confirm no shorts/open on board's electrical net.
- Testing of controlled impedance, using IPC 2141A, on the bare boards will be conducted on a QA sample basis.
- Refer to Table 5: Summary of Tests for complete listing of boards for testing.

3.4 Programming Station

Performed at: The CM

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM

The Master boards must be programmed with current firmware and software revisions, as defined by the BOM, prior to their testing at PCBA FT.

- The CPLD and FLASH may have been programmed prior to their attachment to the bare board with solder paste during board assembly. Programming could be performed with a device programmer on the production line or an outside vendor can deliver preprogrammed CPLD and FLASH to the CM.
- If preprogrammed CPLD and FLASH devices are not available, they must be programmed on board in the following sequence:
    - CPLD – Programming time is approximately 1 to 2 minutes using a PC with an Altera USB Blaster Download Cable connected to the CPLD connector.
    - FLASH Memory – The FLASH Memory will contain the Boot Loader. Programming time is approximately 5 minutes when programming the Flash Memory using JTAG at the CPLD connector. An alternative programming method is using the BDM connector; this will require a Cold Fire Microprocessor Hardware Development kit. Programming time is 5 minutes.
    - After the Cold Fire Microprocessor boots up, an Application program is executed to program the DSP and FPGA devices.
- Once the CPLD and FLASH may have been programmed, the firmware and software revisions may be changed by using a SD card, with the appropriate program, to reflash the CPLD and FLASH memory.

3.5 Automated Optical Inspection (AOI) & Visual Inspection

Performed at: The CM

Test Coverage: Provided by the CM

Implemented by: The CM

Automated Optical Testing shall be performed on populated Printed Circuit Board Assemblies (PCBAs). Visual inspection, per IPC 610, Class 2, will be performed on all boards with fine pitch SMT components.

- Refer to Table 5: Summary of Tests for complete listing of boards for testing.
- CM will provide test coverage report.

3.6 Automated X-Ray Inspection (AXI) Laminography

Performed at: The CM

Test Coverage: Provided by the CM

Implemented by: The CM

Automated X-Ray Laminography shall be performed on populated Printed Circuit Board Assemblies (PCBAs) containing Ball Grid Array (BGA) components where visual inspection is limited. 3-D X-Ray is preferred. From previous Engineering builds, 2-D AXI was not able to detect all unconnected connections on Ball Grid Array devices.

- Master Boards for Wayside, Base, and Locomotive Radios shall require AXI.
- CM will provide test coverage report.

3.7 In-Circuit Test

Performed at: The CM

Test Coverage: Provided by the CM

Implemented by: The CM and possible 3rd party vendor for JTAG

- In-Circuit Testing (ICT) shall be performed on populated Printed Circuit Board Assemblies (PCBAs) to determine shorts/open, wrong components, part orientation, and component value tolerance. Test Jet and Bead Probe technology will be used to increase test coverage.
- Master Boards for Wayside, Base, and Locomotive Radios shall require ICT.
- Boundary Scan tests may be performed at ICT to confirm ICs, with high pin count, to determine shorts/opens and interconnectivity where nail access is limited. These devices include the Coldfire Microprocessor, DSP, FPGA, and CPLD on the Master board.
- ICT may also be used to measure clock frequency, voltage regulation, in-rush current, and perform custom or industry standard built in self tests (BIST) and JTAG.
- ICT fixtures should not apply excessive stress on the board during testing. Using strain gauges attached to board will show excessive stress.

3.8 JTAG and Boundary Scan Station

Performed at: The CM

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM and possible 3rd party vendor for JTAG

- JTAG and Boundary Scan Test will be implemented on a standalone station.
- Master Boards for Wayside, Base, and Locomotive Radio will require Boundary Scan test. These devices include the Coldfire Microprocessor, DSP, FPGA, and CPLD on the Master board.

3.9 PCBA Functional Test (PCBA FT)

Performed at: The CM.

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM and with a possible 3rd party vendor

Board Functional Testing is used to detect parametric faults that are not detectable using static test methods such as ICT. This method of testing typically uses a bed-of-nails test fixture, however, application and measurement of signals should be performed through edge connectors on the circuit board where possible. When not possible, secondary methods such as Test Jet at ICT, AXI, AOI, etc. will be considered to provide QA coverage of these components.

The MTS documentation will provide test limits and pass/fail criteria for the PCBA Functional Tests.

3.9.1 Wayside PCBA Functional Tests

- Master PCBA
  - Verify Power Rail voltages: +1.2V, 1.5V, 1.8V, 2.5V, 5V, 3.3V, 3_3V_PRI, AD_REF, DDS_1.8V, AVDD_3_3, AVDD_3_3_9910B, 1_8ADCIO, 1.8ADC, GPS_LDO_VDD, 3.3V_VS_9517, 3.3V_TCXOBUF, 1.8_TCXO, TCXO_PWR, LNA_V3.0, LMH6517_5V0.
  - Verify Power Rail power-up and power-down sequence (May be done @ ICT)
  - Verify PCBA current draw
  - Verify Reset circuitry: Coldfire/Master Reset, DSP Reset, Power Reset, SPI Device Reset, Power Up/Down Control
  - Verify Power ON Self Test (POST) passes
  - Verify Clocks: Clock Generator, PLL, TCXO, GPS Module, Real Time Clock
  - Verify ColdFire Microprocessor. Verification includes Crystal Oscillator Frequency, CF Comm Port, 64K SPI EEPROM, DSP Debug Com Port, I21C bus devices (Real Time Clock, Clock Generator, Dual MAC, GPS Module), Flex Bus to CPLD, PCI Controller, PLL Test
  - Verify CPLD I/O function: Verification includes A/D Function (VIN, PA_VF, PA_VR, PA_TEMP, 5V, 3.3V, 2.5V, 1.8V, TP15, 1.5V, 1.2V, DGND, 6VS, 3_3V_PRI, 2 spare lines), On Board LEDs, DSP signals, JTAG signals, SD Card, Board Identifier, Watchdog signal to FPGA, Watchdog disable, FPGA Program Port, JTAG Port (TCK, TDO, TDI, TMS), Host Port Interrupt Signals, 8K User Flash Memory (UFM), Flex Bus (FB) to ColdFire
  - Verify Memory: DDR SDRAM, FLASH Memory (Boot Code and Data), Dual MAC Address Memory (2 wire serial memory)

- Verify Ethernet Ports Functionality and LED Indicators: RJ 45 Port 0, RJ 45 Port 1
- Verify SD Card Port: Power to SD Card Reader, Power Current Limit, Read/Write functionality to SD card
- Verify External LEDs activation/deactivation and with displaying correct color: DISPLAY_PWR, DISPLAY_RFLINK, DISPLAY_DTELINK, DISPLAY_STANDBY, DISPLAY_TX, DISPLAY_RX, DISPLAY_FAULT, DISPLAY_VSWR
- Verify DDS-TX Modulator and SAW Filter functionality.
- Verify RX to FPGA circuit functionality. Verification includes RF attenuator, SAW, LNA, ADC amplifier output controlled by FPGA, 14 bit ADC output to FPGA
- Verify FPGA Configuration circuit
- Verify Floating Point DSP circuit: Verification includes DSP/Serial Flash Memory test, DSP/SDRAM test, DSP/FPGA interface test
- Verify DSP Page UHP: Verification includes DSP internal RAM test, 10-bit DAC Octal voltage output test (RSSI 0-1), LED Indicator test, DSP/Coldfire Interface
- Verify Temperature Sensor circuitry
- Temperature Compensated Oscillator (TCXO) calibration.
- Verify signals on connectors

- T-R Switch/LP PCBA
  - Verify Power Rail voltages: 5V
  - Verify PCBA current draw
  - Verify Temperature sensor circuitry
  - Verify Coupler, Forward and Reverse detector functions
  - Verify 161 MHz notch filter and LPF
  - Verify T/R switch function
  - Verify signals on connectors
- RF/DC Power PCBA
  - Verify Power Rail voltages: 5V
  - Verify PCBA current draw
  - Verify PA Bias circuit functionality: Verification includes frequency response, gain, transmit and receive mode operation

- Verify RF Transmitter: Verification includes frequency response (SAW filter and discrete filter), gain, u3-5_5V, transmit and receive mode operation
- Verify signals on connectors

3.9.2 Base/Locomotive Radio PCBA Functional Tests

- Master PCBA – Base/Locomotive Radio
  - Verify Power Rail voltages: 1.2V, 1.5V, 1.8V, 2.5V, 5V, 3.3V, 3_3V_PRI, 6VS, 6V, AD_REF, 1.8V (9910), AVDD_3_3_9910B, 1_8ADCIO, 1.8ADC, GPS_LDO_VDD, VS_9517, 5V_U12, 5V_U31, 3.3_VDC, 5V LDO, U40-5
  - Verify Power Rail power-up and power-down sequence (May be done @ ICT)
  - Verify PCBA current draw
  - Verify Reset circuitry: Coldfire/Master Reset, DSP Reset, Power Reset, SPI Device Reset, Power Up/Down Control
  - Verify Power ON Self Test (POST) passes
  - Verify Clocks: Clock Generator, PLL, TCXO for Loco, OCXO for Base, Real Time Clock, GPS Module (Base Radio Only)
  - Verify ColdFire Microprocessor. Verification includes BDM Connector, CF Comm Port, 64K SPI EEPROM, I21C bus devices (Real Time Clock, Clock Generator, Dual MAC, TACH Monitor), I21C bus external line, Flex Bus to CPLD, PCI Controller, PLL Test, GPS Module (Base Radio Only)
  - Verify CPLD I/O function: Verification includes A/D Function (SENSE28_CONVERTER, 12V_MON, 5V, 3.3V, 2.5V, 1.8V, 1_8V, 1.5V, 1.2V, SENSEMAINS_74_48, TEMP12_CONVERTER, TEMP28_CONVERTER, 2 spare lines), On Board LEDs, DSP signals, JTAG signals, SD Card, Board Identifier, Watchdog signal to FPGA, Watchdog disable, FPGA Program Port, JTAG Port (TCK, TDO, TDI, TMS), Host Port Interrupt Signals, 8K User Flash Memory (UFM), Flex Bus (FB) to ColdFire, Fan Drive/Tach Monitor (Base Radio Only)
  - Verify Memory: DDR SDRAM, FLASH Memory (Boot Code and Data), Dual MAC Address Memory (2 wire serial memory)
  - Verify Ethernet Ports Functionality and LED Indicators: RJ 45 Port 0, RJ 45 Port 1
  - Verify SD Card Port: Power to SD Card Reader, Power Current Limit, Read/Write functionality to SD card

- Verify led Display Board Interface: External LEDs activation/deactivation and with displaying correct color: DISPLAY_PWR, DISPLAY_RFLINK, DISPLAY_DTELINK, DISPLAY_STANDBY, DISPLAY_TX, DISPLAY_RX, DISPLAY_FAULT, DISPLAY_VSWR
- Verify DDS-TX Modulator and SAW Filter functionality, 440 MHz Linear PA LO output
- Verify Modulator Board Interface, TXQ+_980, TXQ-_980, TXI+_980, TXI-_980 outputs
- Verify DCMEAS NULL ADC circuitry, CBUS Interface, Master Connector signals
- Verify Primary/Diversity RX to FPGA circuit functionality. Verification SAW, ADC amplifier output controlled by FPGA, 14 bit ADC output to FPGA
- Verify FPGA Configuration circuit
- Verify Floating Point DSP circuit: Verification includes DSP/Serial Flash Memory test, DSP/SDRAM test, DSP2FPGA SPIO interface test, IQ Modulator SPI port, McASP Interface
- Verify DSP Page UHP: Verification includes DSP internal RAM test, 10-bit DAC Octal voltage output test (RSSI 0-7 & 8-15), LED Indicator test, DSP/Coldfire Interface (Flex Bus), Test DAC, DSP Debug
- Verify Temperature Sensor circuitry
- Verify signals on connectors

- Front End PCBA - Base Radio
  - Verify Power Rail voltages: +5V, 3V3
  - Verify PCBA current draw
  - Verify Transceiver functionality on TX/RX Primary Antenna port. Verification covers 160 MHz Notch filter, T/R Switch & PIN Diode, and LPF circuitry
  - Verify Receiver functionality on TX/RX Primary Antenna port. Verification covers 160 MHz Notch filter, T/R Switch & PIN Diode, LPF, RF switching network, antenna switching network, attenuator, SAW, and LNA circuitry
  - Verify Receiver functionality on RX Primary Antenna port. Verification covers 160 MHz Notch filter, RF switching network, antenna switching network, attenuator, SAW, and LNA circuitry.
  - Verify Receiver functionality on RX Diversity Antenna port. Verification covers 160 MHz Notch filter, RF switching network, attenuator, SAW, and LNA circuitry

- Verify proper signals at board connectors going to: Circulator, Master and PA/Mod boards
- Verify signals on connectors

- Front End PCBA – Locomotive Radio
  - Verify Power Rail voltages: +5V, 3V3
  - Verify PCBA current draw
  - Verify Receiver functionality on Antenna 1 (TX/RX Primary). Verification covers 160 MHz Notch filter, T/R Switch & PIN Diode, LPF, RF switching network, attenuator, SAW, and LNA circuitry
  - Verify Transceiver functionality on Antenna 1 (TX/RX Primary). Verification covers LPF, T/R Switch & PIN Diode, and 160 MHz Notch filter
  - Verify Receiver functionality on Antenna 2 (RX Diversity). Verification covers 160 MHz Notch filter, RF switching network, attenuator, SAW, and LNA circuitry
  - Verify proper signals at board connectors going to: Master and PA/Mod boards
- PA-Mod PCBA – Base/Locomotive Radio
  - Verify Power Rail voltages: +7.15V_PA, 3V3, 3.3V_A, 3V3_D, +5V, A/D_REF
  - Verify PCBA current draw
  - Verify A/D functionality
  - Verify Current Shunt circuitry: Final PA, Driver Stage
  - Verify Temperature sensor circuitry: Final PA, Driver Temp
  - Verify TX_ON digital line
  - Verify proper signals at board connectors going to: Front End, Master, and Power Supply boards.
  - Verify Driver Stage circuitry
  - Verify Final PA circuitry
  - Fixture must provide good electrical ground connection for RF Output Transistor Q1
  - Verify Transmit/Receive functionality on TX/RX Primary Antenna port
  - Verify Receive functionality on RX Diversity Antenna port
  - Calibrate IDQ Current Tune: VR1 potentiometer for final amplifier setting and VR2 potentiometer for driver amplifier setting

  - Verify signals on connectors
- LED PCBA – Base/Locomotive Radio
  - Verify each LED turns ON and OFF
  - Verify each LED display the correct color
  - Verify signals on connectors
- Ethernet PCBA– Base Radio
  - Verify PCBA current draw
  - Verify electrical paths on the two RJ45 and 3.3V connectors
  - Verify termination circuit is present electrically
  - Verify signals on connectors
- Power Supply PCBA – 74V Locomotive Radio, 24V and 48V Base Radio
  - Verify Power Supply current draw
  - Verify 28V Supply regulation with maximum/minimum loads
  - Verify 12V Supply regulation with maximum/minimum loads
  - Verify 12V and 28V output ripple/noise
  - Verify Input Voltage Window Detector function
  - Verify Temperature sensor circuits: 12V and 28V converters
  - Other power supply parameters
  - Verify signals on connectors

3.10 Hipot Test and Ground Bond Test

Performed at: The CM

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM

The purpose of the Hipot test is to ensure a good isolation between the parts of a circuit. Having good isolation helps to guarantee the safety and quality of electrical circuits. Hipot tests are helpful in finding nicked or crushed insulation, stray wire strands or braided shielding, conductive or corrosive contaminants around the conductors, terminal spacing problems, and tolerance errors in IDC cables. All of these conditions might cause a UUT to fail.

The purpose of a Ground Bond test is to ensure any exposed metal on the chassis (screws, connectors, etc.) is electrically connected and can handle high current through the chassis.

The MTS documentation will provide test limits for the Hipot and Ground Bond Tests.

- Wayside Radio: Hipot Testing is not required. Ground Bond Testing is performed on a buttoned up Unit.
- Base Radio: Hipot Testing is not required. Ground Bond Testing is performed on a buttoned up Unit.
- Locomotive Radio: Hipot Testing and Ground Bond Testing are required. Hipot Testing is performed on Unit that has buttoned up after its Calibration/Tuning step. Testing will continue to confirm no damage occurred to the Unit after Hipot Testing.

3.11 Unit Test

Performed at: The CM

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM and possible 3rd party vendor

This test is used to detect interconnect errors between circuit boards and subassemblies, and to detect problems due to interactions between circuits. Calibration steps are also performed to setup the Transmitter RF output and frequency.

The testing at the unit level at the CM site is necessary to find defects not observable at any type of board level testing.

The MTS documentation will provide test limits and pass/fail criteria for the Unit Functional Tests.

3.11.1 Calibration/Tuning

- Wayside Radio Calibration/Tuning
  - The RF/DC Board Bias Level is adjusted for an open loop PA.
  - Output RF power is calibrated.

  - The Peak Envelope Power (PEP) is measured and calibration constants recorded.

- Base/Locomotive Radio Calibration/Tuning

  - An open loop PA check and closed loop PA check is performed to include a quick power on/current draw test and to measure the RF output power with DQPSK modulation transmission.
  - The LO leakage tuning involves tuning the IDC and QDC baseband tuning parameters until the desired LO leakage is achieved. The calibration value is stored in the Master board.
  - The CML phase tuning involves adjusting the CML phase until the desired result is achieved. The calibration value is stored in the Master board.
  - The power output tuning involves adjusting the I and Q gain values until the desired power output is achieved. The calibration value is stored in the Master board.
  - The reference clock tuning involves adjusting the XO setting until the desired relative frequency error is achieved. The calibration value is stored in the Master board.
  - Radio is buttoned up.
  - After Radio is buttoned up (fully assembled), Hipot testing will be performed on Locomotive Radios only.

3.11.2 Functional Tests

- Power consumption
- Communication Ports (E-net)
- GPS receiver interface
- Host Port Interface (HPI)
- I2C
- LED Display
- MAC EEPROM
- PA/MOD board ADC
- SPI interface checkout
- SD-Card interface
- Fan functionality (Base Radio Only)
- Temperature Sensors
- Transmitter Tuning
- Transmitter Output

3.11.3 Radio Transmitter Tests

- Conducted Carrier Output Power
- Carrier Frequency Stability (TCXO calibration(Board))
- Sideband Spectrum
- Adjacent Channel Power Ratio
- Transmitter Current Drain
- Modulation Accuracy / Error Vector Magnitude

3.11.4 Radio Receiver Tests

- Static Reference Sensitivity
- Error Behavior at high input levels

3.12 Stress Screen

Performed at: The CM

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM and possible 3rd party vendor

Stress Screen is a process performed on sub-assemblies and/or completed units to prevent latent (hidden) defects from reaching the customer. These defects typically involve a stress concentrator, which is why they will become Out-of-Box or Early-life (first 90 days) failures. By applying stress (much greater than shipping and initial use), these latent defects get precipitated and become patent (visible) to test. Without stress, they may remain hidden to factory test and be found by customers.

OEM modules may contain latent defects. PCB assemblies may be susceptible to damage from shipping, storage, and handling. Highly stressed components (high voltage or high current) typically do not have huge design margin; they are not able to be sufficiently derated. Variations in strength from batch to batch may cause some weak components to escape into our supply chain. Additionally, manufacturing assembly defects can be inserted by our own processes.

Mechanical defects such as bad solder joints or loose hardware require temperature cycles and/or vibration to exercise them to failure. Electrical

tolerance stack ups and insufficient margins require worst case operational conditions, at elevated temperature. An efficient Stress Screen combines the stresses that target a particular product's susceptibilities.

Stress Screen may include the following tests to the UUT:

- Temperature cycling
- Vibration Testing
- Power Cycling – Verify Power On Self Test passes
- Transmit into RF Load – At maximum power output at CW.
- Receiver testing – Set up to receive data at maximum data rate and check Bit Error Rate (BER).
- GPS Receiver testing
- Exercise SD card reader – Perform read and write cycles at maximum data rate.
- Exercise Ethernet communications at maximum data rate.

3.13 Out of Box Audit (OBA)

Performed at: The CM

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM

The purpose of the OBA is to ensure the unit has gone through all the manufacturing or test process, the unit has passed through all the test process, and the unit is in good quality. The audit may include the following steps:

- Unit checks
    - Confirm unit has passed through the test process.
    - Power up Unit to confirm POST passed.
    - Verify software version and configuration is properly loaded.
    - Verify Ethernet Communication Ports are functional.
    - Verify GPS receiver interface is functional.
    - Verify LED Display is functional
    - Verify correct MAC EEPROM content.

- Verify SD-Card interface functions.
- Verify Fan functionality (Base Radio Only)
- Verify Transmitter operation.
- Verify Receiver operations.
- Verify Labels has been placed in proper location on Unit.
- Verify no cosmetic defects, cracks, and contaminants on unit.
- Verify no rattling of loose components when Unit is shaken.

- Shipping package
  - Items are placed in proper location.
  - Contains correct manuals and documentation.
  - Contains correct accessories, tools, etc.
  - Labels from unit match labels outside of box.

3.14 Ongoing Reliability Test (ORT)

Performed at: The CM

MTS: Owned and written by MCC Test Engineering

Implemented by: The CM and possible 3rd party vendor

The purpose of On-going Reliability Test (ORT) is to identify any adverse changes in the manufacturing process, materials, and/or components by subjecting the product to environmental and mechanical stresses. It will ensure that any changes in process parameters during manufacturing of the product would not adversely affect the functionality and reliability of the product initially or over time. The ORT may also help to expose infant mortality issues due to latent defects by subjecting elevated environmental stresses.

3.14.1 Test Frequency & Sampling Quantity

- Weekly ORT is to provide monitoring of:
  - Product quality: Identify any potential catastrophic product changes, identify any supplier part quality issues.

  - Manufacturing Processes: Identify process deviation early, monitor processes and performance trends over time.
  - Reliability: Validate reliability further down the product life curve.
  - The weekly ORT tests are designed to be set up, cycle tested in an accelerated fashion. Products selected for testing should be representative of the manufacturing process at the time test is performed. All units should be eligible to be returned to inventory. Each unit will be visually inspected and functionally tested prior to the return to inventory.

- Monthly ORT is to provide more in-depth testing:
  - To capture less obvious potential product failures.
  - Provide a test vehicle for more time-consuming, destructive, and qualitative testing.
  - Provide stress tests.
  - Units should be selected randomly from within a specific production time frame. All units should be eligible to be returned to inventory. Each unit will be visually inspected and functionally tested prior to the return to inventory.
- Quarterly ORT is to provide:
  - Validation of basic product specification requirements continue to be met over time.
  - Test product performance in areas not covered in weekly and monthly ORT.
  - Units should be representative of the product at the time of test.
- Yearly ORT is to provide:
  - Verification the products meets Lead Free Product Requirements.
  - Units should be representative of the product at the time of test.

3.14.2 ORT Test Matrix

- The test object in the ORT Test Matrix is to identify any adverse change in manufacturing process, materials, and components.

Table 6: ORT Test Matrix

Tests	Test Description	Test Frequency	Failure Mode
Temperature/Humidity Operational Test	Subject Unit to a temperature/humidity profile for a 24 hour period. Unit is powered and functional during this test.	Weekly	Unit fails to function during test. Cosmetic defects and/or contaminants appear.
Temperature/Humidity Non Operational Test	Unit is subjected to a temperature/humidity profile for a 24 hour period. Unit is powered off during this test.	Weekly	Unit fails to function after test. Cosmetic defects and/or contaminants appear.
Thermal Shock Non Operational Test	Unit is subjected to a Thermal shock profile to simulate worst probable conditions of storage, transportation, and application. Unit is powered off during this test.	Weekly	Unit fails to function after test. Cosmetic defects and/or contaminants appear.
Storage/Shipping Temperature Non Operational Test	Unit is subjected to continuous exposure of the product to high temperatures. Unit is powered off during this test.	Weekly	Unit fails to function after test. Cosmetic defects and/or contaminants appear.
Vibration Non Operational Test	Unit is subjected to a vibration within the predominate or random vibration frequency ranges and magnitudes that may be encountered during the life of the product. Unit is powered off during this test.	Monthly	Unit fails to function after test. Cosmetic defects and/or contaminants appear. Cracks, breakage, internal damage, loose parts or rattling inside unit occurs.

Tests	Test Description	Test Frequency	Failure Mode
Vibration Operational Test	Unit is subjected to a vibration within the predominate or random vibration frequency ranges and magnitudes that may be encountered during the life of the product. Unit is powered and functional during this test.	Monthly	Unit fails to function after test. Cosmetic defects and/or contaminants appear. Cracks, breakage, internal damage, loose parts or rattling inside unit occurs.
Connector Durability Test	Unit is subjected to action of mating and unmating of connectors to simulating expected life of connectors.	Monthly	Unit fails to function after test. After cycling connectors, evaluate wear.
Power Cycling	Unit is subjected to power cycling at elevated temperature and humidity. Unit is powered and functional during this test.	Monthly	Unit fails to function during test. Cosmetic defects and/or contaminants appear.
Drop Operational Test	Unit is subjected to a drop on all surfaces. Unit is powered and functional during this test.	Quarterly	Unit fails to function during test. Cosmetic defects and/or contaminants appear. Cracks, breakage, internal damage, loose parts or rattling inside unit occurs.

Tests	Test Description	Test Frequency	Failure Mode
Drop Non Operational Test	Unit is subjected to a drop on all surfaces. Unit is powered off during this test.	Quarterly	Unit fails to function during test. Cosmetic defects and/or contaminants appear. Cracks, breakage, internal damage, loose parts or rattling inside unit occurs.
Performance Test	Unit is subjected to test where Ethernet connections, Radio Transmitter & Receiver are operating at maximum data rates.	Quarterly	Unit fails to function at maximum data rates during test.
Electrical Test	Unit is subjected to tests Voltage supply corners.	Quarterly	Unit fails to function during test.
RoHS Product Requirement	Use outside vendor to confirm Units produced meet current RoHS requirement.	Yearly	Unit does not meet RoHS requirement.

3.15 Data Base

- Collects all test data in AOI, AXI, ICT, PCBA FT, System FT, Stress Screen, Hipot Test, OBA, and ORT
  - Retrieve test data on a Unit
  - Retrieve test data on a range of dates, lots, etc.
  - Test data can be exported to Excel
- Provides standard analysis
  - Statistical Analysis: Cpk, StdDev, Mean, etc.
  - Histograms
  - Failure Pareto charts
  - First Pass Yields, Second Pass Yields
- Critical Component Lot Codes Tracking to PCBA Serial Numbers
- Board tracking to Radio PN and MAC address
- Integrates with CM Shop Floor Control system

3.16 Test Coverage

100%, structural and functional, distributed across test stations, biased for early detection during the manufacturing flow.

Figure 2: Test/Manufacturing Flow Chart

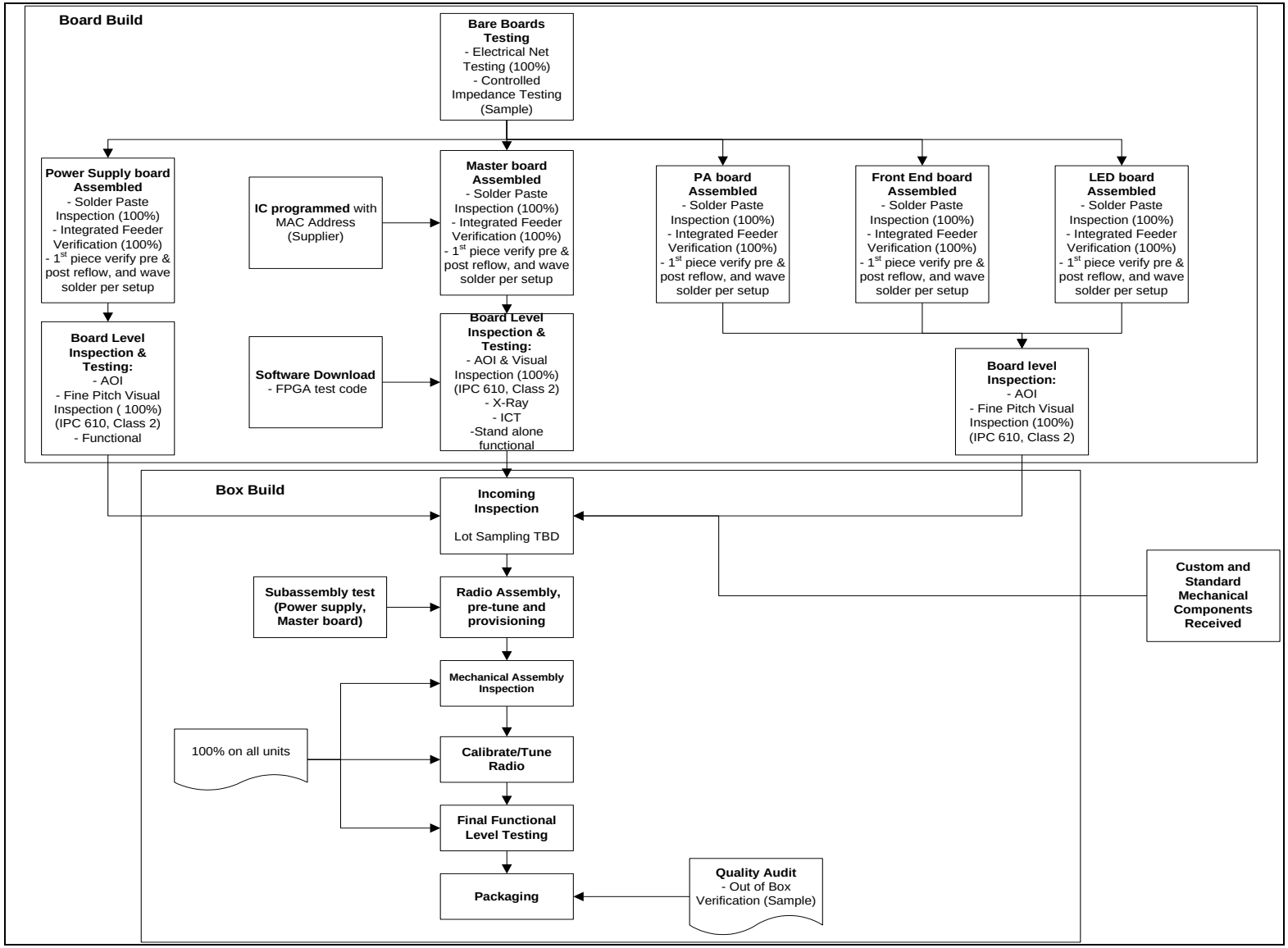


Table 7: Board Build Overview

	Electrical Net Test (100%)	Controlled Impedance (Sample)	Incoming Inspection (Lot Sampling)	Solder Paste Inspection (100%)	Integrated Feeder Verification (100%)	1st Piece Verify (per setup)	AOI (100%)	X-Ray (100%)	ICT (100%)	PWA Functional (100%)	Mechanical Assembly Inspection (100%)	Calibrate/ Tune Radio (100%)	Device Level Functional Test (100%)	System Level Functional Test (100%)	Stress Screen (Sample)	Out of Box Audit (Sample)
All bare PCBs	X	X	X													
PWAs, LBW - Master Boards			X	X	X	X	X	X	X	X					X	
PWAs, LBW – Front End, PA, PS, ENet, LED, LowPass, RF			X	X	X	X	X			X						
Radio Assemblies, LBW											X	X	X	X	X	X
Cycle Time (Minutes)							3	2	4	5	5	5	10	20	30	30